EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S13	34	FPGA with netlist with routing	US-PGPUB; USPAT	OR	OFF	2006/07/20 10:38
S14	0	S13 and dummy	US-PGPUB; USPAT	OR	OFF	2006/07/20 10:30
S15	21	S13 and reduc$8	US-PGPUB; USPAT	OR	OFF	2006/07/20 10:30
S16	1	(FPGA PLA PLD MCM) with netlist with reduc$6	US-PGPUB; USPAT	OR	OFF	2006/07/20 10:39
S17	0	(FPGA PLA PLD MCM) with netlist with simplif$6	US-PGPUB; USPAT	OR	OFF	2006/07/20 10:40
S18	6	(FPGA PLA PLD MCM) with netlist with siz$3	US-PGPUB; USPAT	OR	OFF	2006/07/20 10:42
S19	3	(FPGA PLA PLD MCM) with netlist with CLB	US-PGPUB; USPAT	OR	OFF	2006/07/20 10:42

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	0	FPGA with netlist with CLB with bypass	US-PGPUB; USPAT	OR	OFF	2006/07/20 16:45
L4	0	FPGA with netlist with (bypass feedthrough)	US-PGPUB; USPAT	OR	OFF	2006/07/20 16:44
L5	0	FPGA with netlist with ((by adj pass) feedthrough)	US-PGPUB; USPAT	OR	OFF	2006/07/20 16:44
L6	278	FPGA with netlist	US-PGPUB; USPAT	OR	OFF	2006/07/20 16:45
L7	3	FPGA with netlist with CLB	US-PGPUB; USPAT	OR	OFF	2006/07/20 16:50
L8	1	"6134516".pn.	US-PGPUB; USPAT	OR	OFF	2006/07/20 16:50

Google Remove items from Search History (Beta) for AXSaxena@gmail.com

Search History
- Web
- Images
- News
- Froogle
- Video

Select all
Pause
Remove Items

Trends

Bookmarks
- Unlabeled (1)

Add bookmark

Remove Cancel Select: All, None | Clear entire Search History »

Jul 20, 2006

- "FPGA netlist" CLB feed-through
- "FPGA netlist" CLB feed through
  - Simulation server system and method - Patent 6134516
    freepatentsonline.com/6134516.html
- "FPGA netlist" CLB feedthrough
- "FPGA netlist" CLB bypass
  - Xilinx DS099 Spartan-3 FPGA Family Complete Data Sheet
    inf.ntb.ch/.../Spartan/pdfs/SpartanIII_Datasheet.pdf
  - Xilinx/ Synopsys Interface Guide
    www.xilinx.com/support/sw_manuals/2_1i/download/xsi_int.pdf
- "FPGA netlist" modified netlist
  - Introduction: Philips requirement SAME 2004
    www.eve-team.com/pdf/Art32.pdf
  - A Methodology for FPGA to Structured-ASIC Synthesis and Verification - 2 visits
    portal.acm.org/ft_gateway.cfm?id=1131369&type=pdf&a...
- "FPGA netlist" size reduction bypass
  - Augmenting a Microprocessor with Reconfigurable Hardware by John ...
    brass.cs.berkeley.edu/documents/AugmentingProcWithRecon...
  - Automating Layout of Reconfigurable Subsystems for
    www.ee.washington.edu/.../phillips_dissertation_2004.pdf
  - EDN Access--11.20.97 Moving beyond programmable logic: If, when, how?
    www.edn.com/archives/1997/112097/24df_02.htm
  - PowerPoint Presentation
    www.flextronicssemi.com/FlexSemiSoCCapabilities.pdf
- "FPGA netlist" size reduction
  - A Methodology for FPGA to Structured-ASIC Synthesis and Verification - 2 visits
    portal.acm.org/ft_gateway.cfm?id=1131369&type=pdf&a...
- "FPGA netlist"
- "FPGA netlist" reduction dummy CLB
- dummy CLB netlist reduction

Remove Cancel Select: All, None | Clear entire Search History »

Terms used **FPGA netlist reduction**

Found **2,959** of **182,223**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 A hierarchy-driven FPGA partitioning method

Helena Krupnova, Ali Abbara, Gabrièle Saucier

June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**

Publisher: ACM Press

Full text available: pdf(50.71 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

This paper addresses an automatic partitioning method of adesign into several FPGAs. Although the circuit partitioningmethods have recently been significantly advanced, partitioningis commonly performed at the gate netlist level. To cope withlarge designs and explore the solution space efficiently,clustering of the logic is mandatory. In this paper, the hierarchyof the design, naturally introduced by the designer, guides thepartitioning. The basic concepts are introduced in terms of"envelope" de ...

2 Poster session IV: Evaluation of dual V_{DD} fabrics for low power FPGAs

Rajarshi Mukherjee, Seda Ogrenci Memik

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(531.02 KB) Additional Information: full citation, abstract, references

Power efficiency is becoming an increasingly important design aspect for FPGAs. Recently it has been shown that well-known power minimization techniques in the ASICs such as creating supply voltage (Vdd) scalable islands of different granularity can be applied to FPGAs. However, the discrete routing architecture of FPGAs amplifies any constraint imposed on the placement stage. In this work, we evaluate the overheads of voltage scaling schemes in relation to FPGA architectures and desi ...

3 CAD for FPGAs: Multiplexer restructuring for FPGA implementation cost reduction

Paul Metzgen, Dominic Nancekievill

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(691.28 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a novel synthesis algorithm that reduces the area needed for implementing multiplexers on an FPGA by an average of 18%. This is achieved by reducing the number of Lookup Tables (LUTs) needed to implement multiplexers. The algorithm relies on reimplementing 2:1 multiplexer trees using efficient 4:1 multiplexers. The key to the algorithm's performance lies in exploiting the observation that most multiplexers occur in busses. New optimizations are employed which pay a small cost ...

Keywords: FPGA, busses, logic optimization, multiplexers, recoding, restructuring, synthesis

4 PROP: a recursive paradigm for area-efficient and performance oriented partitioning of large FPGA netlists

Roman Kužnar, Franc Brglez

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(389.16 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

In this paper, we introduce a new recursive partitioning paradigm PROP which combines (p)artitioning, (r)eplication, (o)ptimization, to be followed by another recursion of (p) artitioning, etc. We measure the quality of partitions in terms of total device cost, logic and terminal utilization, and critical path delay. Traditionally, the minimum lower bound into which a given netlist can be partitioned is determined by disregarding the logic interconnect while distributing the logic nodes into a mi ...

Keywords: partitioning, FPGA, optimization, resynthesis, critical path delay

5 Architectures: Exploration of pipelined FPGA interconnect structures

Akshay Sharma, Katherine Compton, Carl Ebeling, Scott Hauck

February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(336.73 KB) Additional Information: full citation, abstract, references, index terms

In this work, we parameterize and explore the interconnect structure of *pipelined* FPGAs. Specifically, we explore the effects of interconnect register population, length of registered routing track segments, registered IO terminals of logic units, and the flexibility of the interconnect structure on the performance of a pipelined FPGA. Our experiments with the RaPiD [4] architecture identify tradeoffs that must be made while designing the interconnect structure of a pipelined FPGA. The po ...

Keywords: PipeRoute, architecture explorations, pipelined FPGA, pipelined interconnect, registered routing

6 CAD 1: Improvements to technology mapping for LUT-based FPGAs

Alan Mishchenko, Satrajit Chatterjee, Robert Brayton

February 2006 **Proceedings of the internation symposium on Field programmable gate arrays FPGA'06**

Publisher: ACM Press

Full text available: pdf(152.84 KB) Additional Information: full citation, abstract, references, index terms

The paper presents several improvements to state-of-the-art in FPGA technology mapping exemplified by a recent advanced technology mapper DAOmap [Chen and Cong, ICCAD '04]. Improved cut enumeration computes all K-feasible cuts without pruning for up to 7 inputs for the largest MCNC benchmarks. A new technique for on-the-fly cut dropping reduces by orders of magnitude memory needed to represent cuts for large designs. Improved area recovery leads to mappings with area on average 7% smaller than D ...

Keywords: FPGA, area recovery, cut enumeration, lossless synthesis, technology mapping

7 On the Interaction Between Power-Aware FPGA CAD Algorithms

Julien Lamoureux, Steven J. E. Wilton

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(178.73 KB) Additional Information: full citation, abstract, citings, index terms

As Field-Programmable Gate Array (FPGA) power consumptioncontinues to increase, lower power FPGA circuitry, architectures,and Computer-Aided Design (CAD) tools need to be developed.Before designing low-power FPGA circuitry, architectures, orCAD tools, we must first determine where the biggest savings (interms of energy dissipation) are to be made and whether thesesavings are cumulative. In this paper, we focus on FPGA CADtools. Specifically, we describe a new power-aware CAD flow forFPGAs that w ...

8 Architecture analysis and automation: Architecture evaluation for power-efficient FPGAs

Fei Li, Deming Chen, Lei He, Jason Cong

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(338.83 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a flexible FPGA architecture evaluation framework, named fpgaEVA-LP, for power efficiency analysis of LUT-based FPGA architectures. Our work has several contributions: (i) We develop a mixed-level FPGA power model that combines switch-level models for interconnects and macromodels for LUTs; (ii) We develop a tool that automatically generates a back-annotated gate-level netlist with post-layout extracted capacitances and delays; (iii) We develop a cycle-accurate power simulato ...

Keywords: FPGA architecture, FPGA power model, low power design

9 FPGA circuit design and layout: Power modeling and architecture evaluation for FPGA with novel circuits for Vdd programmability

Yan Lin, Fei Li, Lei He

February 2005 **Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(365.92 KB) Additional Information: full citation, abstract, references, index terms

Vdd-programmable FPGAs have been proposed recently to reduce FPGA power, where Vdd levels can be customized for different circuit elements and unused circuit elements can be power-gated. In this paper, we first develop an accurate FPGA power model and then design novel Vdd-programmable interconnect switches with minimum number of configuration SRAM cells. Applying our power model to placed and routed benchmark circuits, we evaluate Vdd-programmable FPGA architecture using the new switches. The b ...

Keywords: FPGA architecture, FPGA power model, Vdd programmability, dual-Vdd, low power

10 I/O and performance tradeoffs with the FunctionBus during multi-FPGA partitioning

Frank Vahid

February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(1.26 MB) Additional Information: full citation, references, citings, index terms

11 Session 4: Partitioning & Placement: Fine granularity clustering for large scale placement problems

Bo Hu, Malgorzata Marek-Sadowska

April 2003 **Proceedings of the 2003 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(246.45 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a linear-time Fine Granularity Clustering (FGC) algorithm to

reduce the size of large scale placement problems. FGC absorbs as many nets as possible into Fine Clusters. The absorbed nets are expected to be short in any good placement; therefore the clustering process does not affect the quality of results. We compare FGC with a connectivity-based clustering algorithm proposed in [1] and simulated-annealing-based algorithm in TimberWolf [2], both of which also reduce the ... .

Keywords: clustering, placement

12 Timing optimization: Techniques for improved placement-coupled logic replication

Hosung (Leo) Kim, John Lillis, Miloš Hrkić, Miloš Hrkić
April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**
Publisher: ACM Press
Full text available: pdf(282.17 KB) Additional Information: full citation, abstract, references, index terms

Several recent papers have utilized logic replication driven by placement-level timing analysis for improving clock period (e.g., [1], [8], [18], and [2]). All of these papers demonstrated, through various optimization strategies, the potential of the basic technique of replication. In this paper we propose a number of techniques aimed at more fully realizing this potential within the framework employed in [8]. As reported in [7], there are situations in which the approach of [8] fails to yield ...

Keywords: logic replication, placement, programmable logic, timing optimization

13 Physical Design: Efficient circuit clustering for area and power reduction in FPGAs

Amit Singh, Malgorzata Marek-Sadowska
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(935.90 KB) Additional Information: full citation, abstract, references, citings

We present a routability-driven bottom-up clustering technique for area and power reduction in clustered FPGAs. This technique uses a cell connectivity metric to identify seeds for efficient clustering. Effective seed selection, coupled with an interconnect-resource aware clustering and placement, can have a favorable impact on circuit routability. It leads to better device utilization, savings in area, and reduction in power consumption. Routing area reduction of 35% is achieved over previously ...

14 Extra-dimensional island-style FPGAs (abstract only)

Herman Schmit
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(102.29 KB) Additional Information: full citation, index terms

15 Exploiting early partial reconfiguration of run-time reconfigurable FPGAs in embedded systems design (abstract only)

Byoungil Jeong, Sungjoo Yoo, Kiyoung Choi
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(102.29 KB) Additional Information: full citation, index terms

16 Efficient support of hardware debugging through FPGA physical design partitioning

John Lach, William H. Mangione-Smith, Miodrag Potkonjak
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**
Publisher: ACM Press

Full text available: pdf(102.29 KB) Additional Information: full citation, index terms

17 Technology mapping for FPGAs with nonuniform pin delays and fast interconnections

Jason Cong, Yean-Yow Hwang, Songjie Xu

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Publisher: ACM Press

Full text available: pdf(819.54 KB) Additional Information: full citation, references, citings, index terms

18 Synthesis and floorplanning for large hierarchical FPGAs

H. Krupnova, C. Rabedaoro, G. Saucier

February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(1.10 MB) Additional Information: full citation, references, citings, index terms

19 Placement: Hardware-assisted simulated annealing with application for fast FPGA placement

Michael G. Wrighton, André M. DeHon

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(503.33 KB) Additional Information: full citation, abstract, references, citings, index terms

To truly exploit FPGAs for rapid turn-around development and prototyping, placement times must be reduced to seconds; late-bound, reconfigurable computing applications may demand placement times as short as microseconds. In this paper, we show how a systolic structure can accelerate placement by assigning one processing element to each possible location for an FPGA LUT from a design netlist. We demonstrate that our technique approaches the same quality point as traditional simulated annealing as ...

Keywords: design automation, field-programmable gate arrays, placement, reconfigurable computing, simulated annealing

20 Reconfigurable computing: A methodology for FPGA to structured-ASIC synthesis and verification

Mike Hutton, Richard Yuan, Jay Schleicher, Gregg Baeckler, Sammy Cheung, Kar Keng Chua, Hee Kong Phoo

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Designers' forum DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(246.06 KB) Additional Information: full citation, abstract, references

Structured-ASIC design provides a mid-way point between FPGA and cell-based ASIC design for performance, area and power, but suffers from the same increasing verification burden associated with cell-based design. In this paper we address the verification issue with a methodology and fabric to directly tie FPGA prototype and functional in-system verification with a clean migration path to structured ASIC. The most important aspects of this methodology are the use of physically identical blocks fo ...

Thu, 20 Jul 2006, 2:32:40 PM EST

Edit an existing query or compose a new query in the Search Query Display.

Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Search Query Display

[redacted]

Recent Search Queries		Results
#1	((fpga<in>metadata) <and> (netlist<in>metadata))<and> (compaction<in>metadata)	0
#2	((fpga<in>metadata) <and> (netlist<in>metadata))<and> (reduction<in>metadata)	1
#3	((reconfigurable <in>metadata) <and> (netlist<in>metadata)) <and> (reduction<in>metadata)	0
#4	((fpga<in>metadata) <and> (netlist<in>metadata))	53
#5	((clb<in>metadata) <and> (netlist<in>metadata))	2
#6	((clb<in>metadata) <and> (fpga<in>metadata))<and> (optimize<in>metadata)	8
#7	((fpga<in>metadata) <and> (netlist<in>metadata))<and> (reduced<in>metadata)	8
#8	((clb<in>metadata) <and> (configuration<in>metadata)) <and> (fpga<in>metadata)	18
#9	((clb <in>metadata) <and> (configuration<in>metadata)) <and> (optimization<in>metadata)	1
#10	((clb<in>metadata) <and> (feedthrough<in>metadata)) <and> (fpga<in>metadata)	0
#11	((clb<in>metadata) <and> (feedthrough<in>metadata))	0
#12	((fpga <in>metadata) <and> (feedthrough<in>metadata))	0
#13	((fpga<in>metadata) <and> (clb<in>metadata))<and> (bypass<in>metadata)	1

[redacted]

Results for "(((fpga or pragrammable logic array) and netlist and reduction)<in>metadata)" e-mail
Your search matched 1 of 1373978 documents.
A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

New Search

Modify Search

(((fpga or pragrammable logic array) and netlist and reduction)<in>metadata) Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **PROP: a recursive paradigm for area-efficient and performance oriented large FPGA netlists**
Kuznar, R.; Brglez, F.;
Computer-Aided Design, 1995. ICCAD-95. Digest of Technical Papers., 1995 I International Conference on
5-9 Nov. 1995 Page(s):644 - 649
Digital Object Identifier 10.1109/ICCAD.1995.480197
AbstractPlus | Full Text: PDF(788 KB) IEEE CNF
Rights and Permissions